F1024/F1280

Uncooled Thermal Imaging Module

User Expansion Component Manual

V1.0.0

Version History

Version	Date	Description
V1.0.0	2024-08	Initial release

Table of Contents

1 User Expansion Component 01/11

The User Expansion Component 01 is compatible with 1024 and 1280 uncooled thermal imaging modules. This component includes 5 connectors, as shown in Figure 1.1, and supports interfaces such as BT601/BT1120 output, RS232, RS485, external sync, alarm, and motor control. Interface definitions are shown in the accompanying diagram. It also includes standard wiring cables. For detailed descriptions, refer to Sections 1.1 to 1.5.

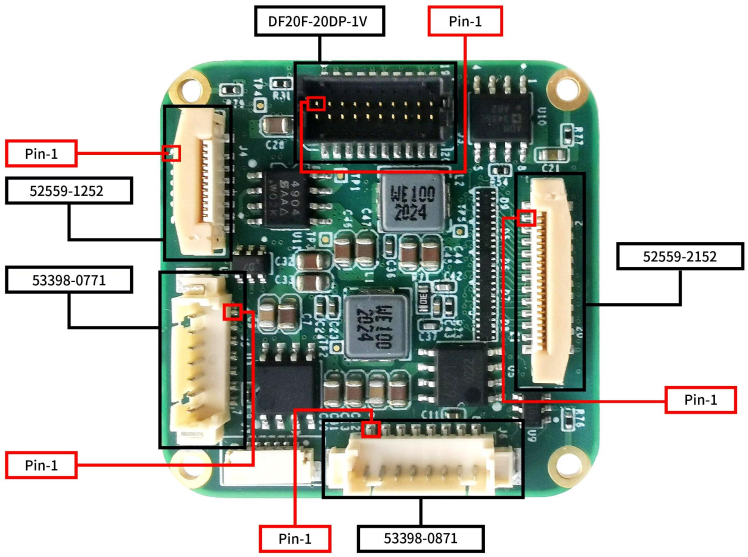

Figure1.1 Expansion Component 01 (For F1024 Modules)

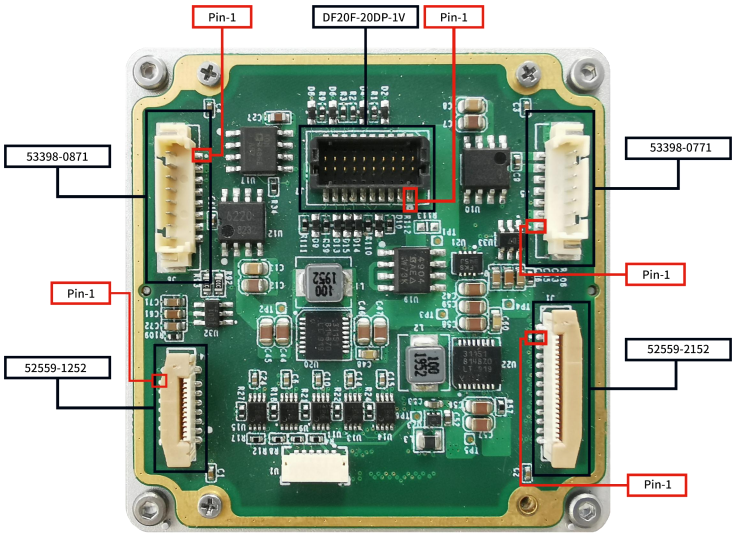

Figure1.2 Expansion Component 01/11 (For F1280 Modules)

1.1 Zoom Motor Control Socket

The zoom motor control uses a MOLEX 53398-0771 7-pin connector, providing interfaces for lens zoom motor drive, zoom potentiometer drive, and signal acquisition. The socket pinout is detailed in Table 1.1.

Table1.1 The Interface Definition of MOLEX 53398-0771

PIN NO.	PIN Name	Type	Description
1	+12V_OUT	Power	Power Output 12V
2	GND	Power	Power Ground
3	ZOOM_VOLTAGE	Input	Feedback of Zoom Potentiometer
4	NULL	/	NC
5	NULL	/	NC
6	ZOOM_MOTOR+	Output	Motor Output Positive Terminal (12V)
7	ZOOM_MOTOR-	Output	Motor Output Negative Terminal

1.2 Focus Motor Control Socket

The focus motor control socket uses MOLEX 53398-0871 8-pin connector, providing connections for the lens focus motor drive, focus potentiometer drive, and signal acquisition interface. The socket interface definitions are as shown in Table 1.2.

Table1.2 The Interface Definition of 53398-0871

PIN NO.	PIN Name	Type	Description
1	+12V_OUT	Power	Power Output 12V
2	GND	Power	Power Ground
3	FOCUS_VOLTAGE	Input	Feedback of Focusing potentiometer
4	NULL	/	NC
5	NULL	/	NC
6	FOCUS_MOTOR+	Output	Motor Output + (12V)
7	FOCUS_MOTOR-	Output	Motor Output -
8	NULL	/	NC

1.3 Parallel Digital Video Socket

The parallel digital video socket uses MOLEX 52559-2152 21-pin connector, supporting BT.1120 and LVCMOS digital video output. The socket interface definitions are as shown in Table 1.3.

Table1.3 The Interface Definition of MOLEX 52559-2152

PIN NO.	PIN Name	Type	Description
1	DV1	Output	BT.656/BT.1120/LVCMOS digital signal1
2	DV0	Output	BT.656/BT.1120/LVCMOS digital signal 0
3	DV3	Output	BT.656/BT.1120/LVCMOS digital signal 3
4	DV2	Output	BT.656/BT.1120/LVCMOS digital signal 2
5	DV5	Output	BT.656/BT.1120/LVCMOS digital signal 5
6	DV4	Output	BT.656/BT.1120/LVCMOS digital signal 4
7	DV7	Output	BT.656/BT.1120/LVCMOS digital signal 7
8	DV6	Output	BT.656/BT.1120/LVCMOS digital signal 6
9	DV9	Output	BT.1120/LVCMOS digital signal 9
10	DV8	Output	BT.1120/LVCMOS digital signal 8
11	DV11	Output	BT.1120/LVCMOS digital signal 11
12	DV10	Output	BT.1120/LVCMOS digital signal 10
13	DV13	Output	BT.1120/LVCMOS digital signal 13
14	DV12	Output	BT.1120/LVCMOS digital signal 12
15	DV15	Output	BT.1120 digital signal 15
16	DV14	Output	BT.1120 digital signal 14
17	GND	Power	Power Ground
18	DV_VSYNC	Output	Frame valid signal
19	DV_HSYNC	Output	Row valid signal
20	GND	Power	Power Ground
21	DV_CLK	----	Clock signal

1.4 Differential Digital Video Socket

The differential digital video output socket uses MOLEX 52559-1252 12-pin connector, providing LVDS digital video output. The socket interface definitions are as shown in Table 1.4.

Table1.4 The Definition of MOLEX 52559-1252 12-pin Connector

PIN NO.	PIN Name	Type	Type
1	LVDS_CLK+	Output	LVDS_H CLK Signal
2	LVDS_CLK-	Output	
3	GND	Power	Power Ground
4	LVDS_DATA1+	Output	LVDS_H Digital Signal 1
5	LVDS_DATA1-	Output	
6	LVDS_DATA2+	Output	LVDS_H Digital Signal 2

7	LVDS_DATA2-	Output	
8	LVDS_DATA3+	Output	LVDS_H Digital Signal 3
9	LVDS_DATA3-	Output	
10	LVDS_DATA4+	Output	LVDS_H Digital Signal 4
11	LVDS_DATA4-	Output	
12	GND	Power	Power Ground

1.5 Power Serial Port Socket

The power serial port uses an HRS DF20F-20DP-1V 20-pin socket, supporting 5~24V DC power supply, one RS232 serial communication interface, one RS485 serial communication interface, one UART serial communication interface, four button control interfaces, one synchronous input interface, one synchronous output interface, and one alarm I/O output. The socket interface definitions are as shown in Table 1.5.

Table1.5 The Interface Definition of HRS DF20F-20DP-1H

PIN No.	PIN Name	Type	Description
1	GND	Power	Power Ground
2	POWER_IN	Power	Power In (5~24-DC)
3	GND	Power	Power Ground
4	POWER_IN	Power	Power In (5~24-DC)
5	RS232_RX	In	RS232 Serial Input Interface
6	GND	Power	Power Ground
7	RS232_TX	Out	RS232 Serial Output Interface
8	RS485-	In/Out	RS485 Serial Input/Output Interface (PTZ Control)
9	GND	Power	Power Ground
10	RS485+	In/Out	RS485 Serial Input/Output Interface (PTZ Control)
11	SYNC_IN	In	External Sync Input Interface
12	KEY1	In	Button (C)
13	NC	In	Reserved
14	KEY2	In	Button(-)
15	NC	Out	Reserved
16	KEY3	In	Button (+)
17	ALARM	Out	Alarm output IO, high-low level (3.3V)
18	KEY4	In	Button (M)
19	SYNC_OUT	Out	External Sync Output Interface
20	NULL	In	Reserved

2. User Expansion Component Ethernet 18/28

The user expansion component is suitable for 1024 and 1280 uncooled thermal imaging modules. This user component contains 5 sockets, as shown in Figures 2.1 and 2.2, supporting power input, RS-485, network, alarm input/output, audio input/output, and other interfaces. The interface definitions are as shown in the figures.

2.1 User Expansion Component Ethernet 18 For F1024 Modules

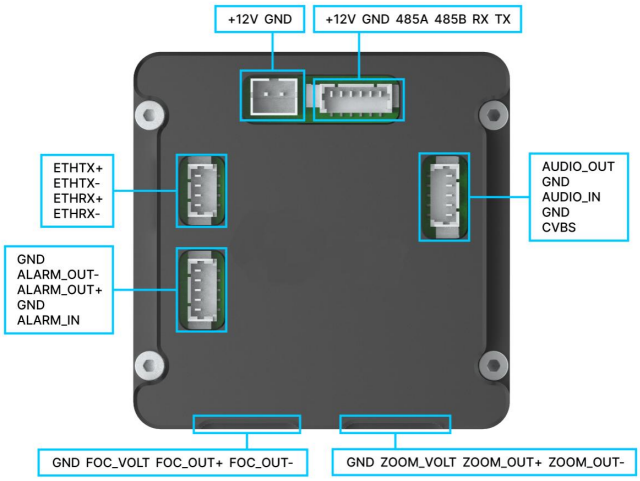

Figure 2.1 User Expansion Component Ethernet 18 For F1024 Modules

2.2 User Expansion Component Ethernet 28 For F1280 Modules

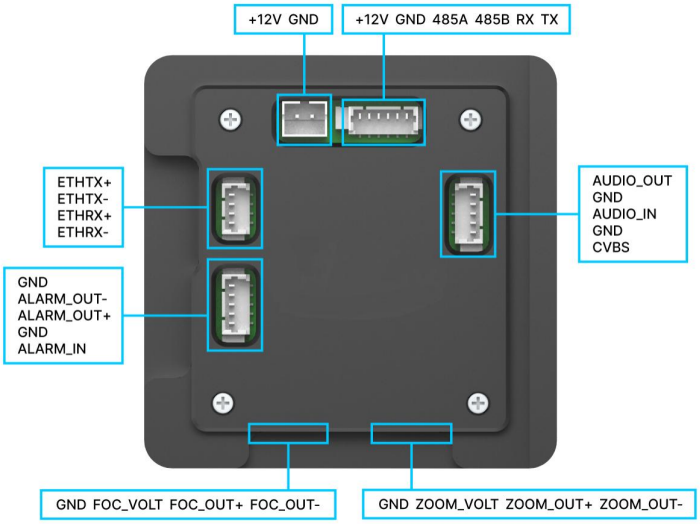

Figure 2.2 User Expansion Component Ethernet 28 For F1280 Modules

3. User Expansion Component 09 SDI

The 09 SDI user expansion component is suitable for 1024 and 1280 thermal imaging modules, containing 4 sockets, as shown in Figures 3.1 and 3.2. It supports SDI, power input, RS232, RS485, external synchronization, alarm, motor control, and other interfaces. Specific descriptions can be found in sections 3.1 to 3.5.

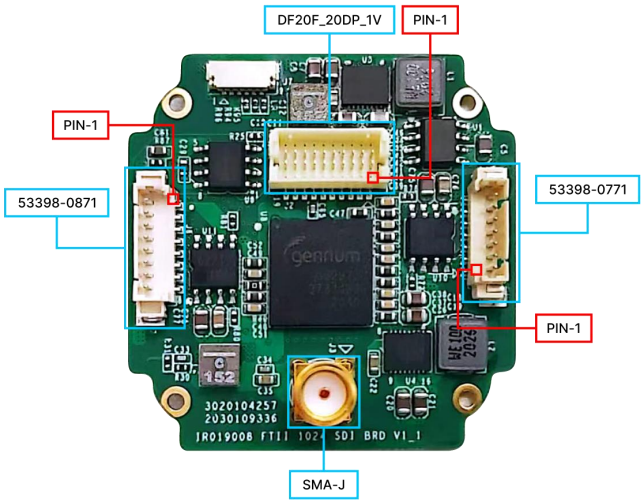

Figure 3.1 User Expansion Component 09 SDI For F1024 Modules

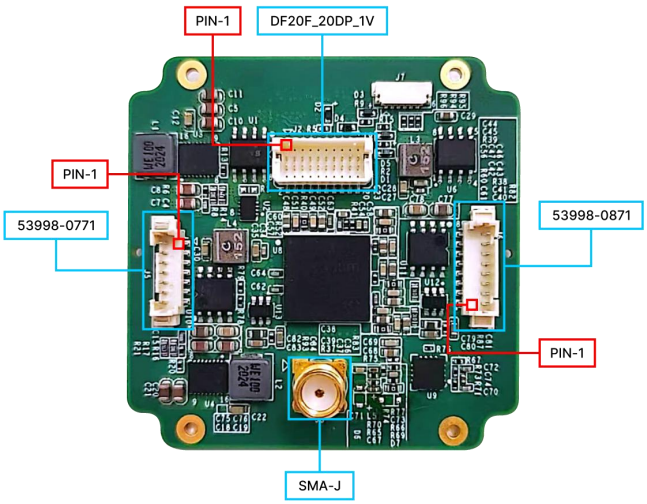

Figure 3.2 User Expansion Component 09 SDI For F1280 Modules

3.1 Zoom Motor Control Socket

The zoom motor control socket uses a MOLEX 7-pin connector, providing connections for the lens zoom motor drive, zoom potentiometer drive, and signal acquisition interface. The socket interface definitions are as shown in Table 3.1.

Table 3.1 Definition of 53398-0771 7-pin Socket

Pin No.	Pin Name	Type	Descriptions
1	+12V_OUT	Power	12V output
2	GND	Power	Power GND
3	ZOOM_VOLTAGE	Input	Feedback of zoom potentiometer
4	NULL	----	NC
5	NULL	----	NC
6	ZOOM_MOTOR+	Output	Motor output + (12V)
7	ZOOM_MOTOR-	Output	Motor output -

3.2 Focus Motor Control Socket

The focus motor control socket uses an 8-pin MOLEX connector, providing connections for the lens focus motor drive, focus potentiometer drive, and signal acquisition interface. The socket interface definitions are as shown in Table 3.2.

Table 3.2 Definition of 53398-0871 8-pin Socket

Pin No.	Pin Name	Type	Descriptions
1	+12V_OUT	Power	12V output
2	GND	Power	Power GND
3	FOCUS_VOLTAGE	Input	Feedback of zoom potentiometer
4	NULL	----	Not connected
5	NULL	----	Not connected
6	FOCUS_MOTOR+	Output	Motor output + (12V)
7	FOCUS_MOTOR-	Output	Motor output-
8	NULL	----	Not connected

3.3 Power Serial Port Socket

The power serial port uses an HRS DF20F-20DP-1V 20-pin connector, supporting 5~24V DC power supply, one RS232 serial communication interface, one RS485 serial communication interface, one UART serial communication interface, one synchronous input interface, one synchronous output interface, and one alarm I/O output. The socket interface definitions are as shown in Table 3.3.

Table 3.3 The Definition of 20-pin HRS DF20F-20DP-1V

Pin No.	Pin Name	Type	Descriptions
1	GND	Power	Power GND
2	POWER_IN	Power	Power Input (5~24-DC)
3	GND	Power	Power GND
4	POWER_IN	Power	Power Input (5~24-DC)
5	RS232_RX	Input	RS232 serial input interface
6	GND	Power	GND
7	RS232_TX	Output	RS232 serial output interface
8	RS485-	Input & Output	RS485 serial input output interface (PT control)
9	GND	Power	Power GND
10	RS485+	Input & Output	RS485 serial input output interface (PT control)
11	SYNC_IN	Input	External sync input
12	NC	Input	Reserved
13	NC	Input	Reserved
14	NC	Input	Reserved
15	NC	Output	Reserved
16	NC	Input	Reserved
17	ALARM	Output	Alarm output IO, high and low level (3.3V)
18	NC	Input	Reserved
19	SYNC_OUT	Output	External sync output
20	NC	Input	Reserved

3.4 SDI Socket

SDI uses an SMA-J connector, providing SDI digital video output.

4. Description of Accessory Board

The accessory board is used to extend the function of digital expansion board, the digital video can be converted to HDMI, USB, CameraLink format by adding the accessory board.

4.1 HDMI Accessory Board

The HDMI accessory board is compatible with F1024 and F1280 thermal imaging modules.

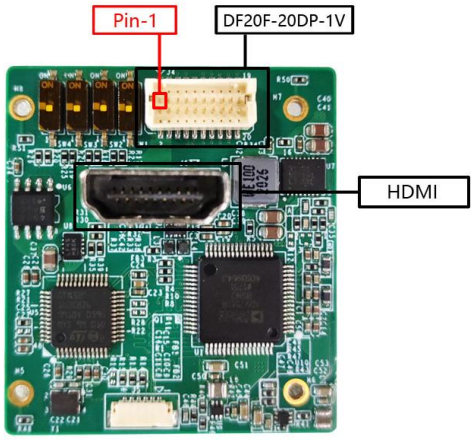

Figure 4.1 HDMI Accessory Board

The 20-pin HRSDF20F-20DP-1V socket supports 5～24V DC power supply, 1-channel RS232 serial communication interface, 1-channel RS-485 serial communication interface, 1-channel sync input interface, 1-channel sync output interface and 1-channel alarm output. Refer to Table 3.3 for detailed information.

4.2 USB Accessory Board

The USB accessory board is compatible with four models: F1024 and F1280 thermal imaging modules.

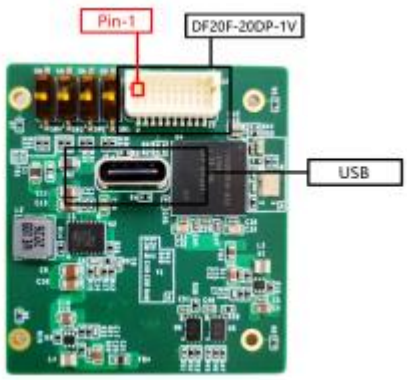

Figure 4.2 USB Accessory Board

The 20-pin HRSDF20F-20DP-1V socket supports 5~24V DC power supply, 1-channel RS232 serial communication interface, 1-channel RS-485 serial communication interface, 1-channel sync input interface, 1-channel sync output interface and 1-channel alarm output. Refer to Table 3.3 for detailed descriptions.

4.3 Cameralink Accessory Board

The Cameralink accessory board is compatible with four models: F1024 and F1280 thermal imaging modules.

Figure 4.3 Cameralink Accessory Board

The 20-pin HRSDF20F-20DP-1V socket supports 5～24V DC power supply, 1-channel RS232 serial communication interface, 1-channel RS-485 serial communication interface, 1-channel sync input interface, 1-channel sync output interface and 1-channel alarm output. Refer to Table 1.3 for detailed descriptions.

5. Introduction of Digital Video Format

5.1 LVCMOS Video Format

The LVCMOS digital video signals contain one clock signal (Clock), one frame valid signal, one line valid signal, fourteen data signals (DV0-DV13). When one frame data comes, the frame synchronizing signal is set high level, which indicates that the following data belongs to the same frame. After this frame data is finished, the frame synchronizing signal is set low level, which indicates that this frame data is finished; For the same reason, when one line data comes, the line synchronizing signal is set high level, after this line of data is finished, the line synchronizing signal is set low level. Refer to the following Figure 5.1 for the sequence chart of LVCMOS video:

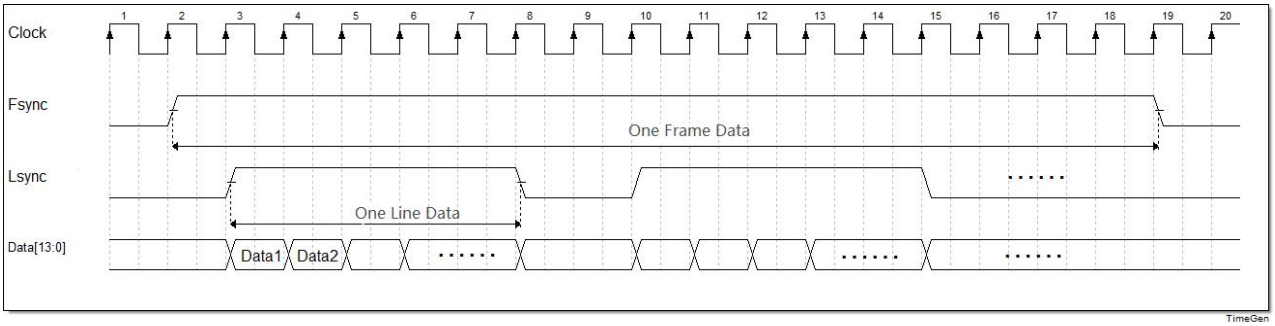

Figure 5.1 LVCMOS Timing

Users can choose the ORG(original) data, NUC(Non-uniformity Correction) data, DNS(image denoising) data and DRC(image processing) data for LVCMOS data source. For the above data source, except that every pixel for DRC data is 10bit, the pixel for other data sources is 14 bit; in the above figure, the synchronizing signal and data signal are all changed on the clock rising edge. In order to make sampling on the rising edge of clock, the signal can be changed on the falling edge of the clock in actual program design.

Table 5.1 LVCMOS CLK Frequency

Model	CLK Frequency
1024	35MHz
1280	90.000MHz

5.2 BT.1120 Video Format

There are two kinds of BT.1120 digital video timing for uncooled thermal imaging cores, internal sync and external sync. Internal sync adopts sync reference number to indicate the start and end of every line or every frame, 16 data lines and one clock line are included. Besides 16 data lines and one clock line in external sync, one line sync signal and one field sync signal are also included. The default BT1120 video source is DRC and it can not be changed.

5.2.1 Timing Introduction of External Sync

See the following Figure 5.2 for timing chart of external sync:

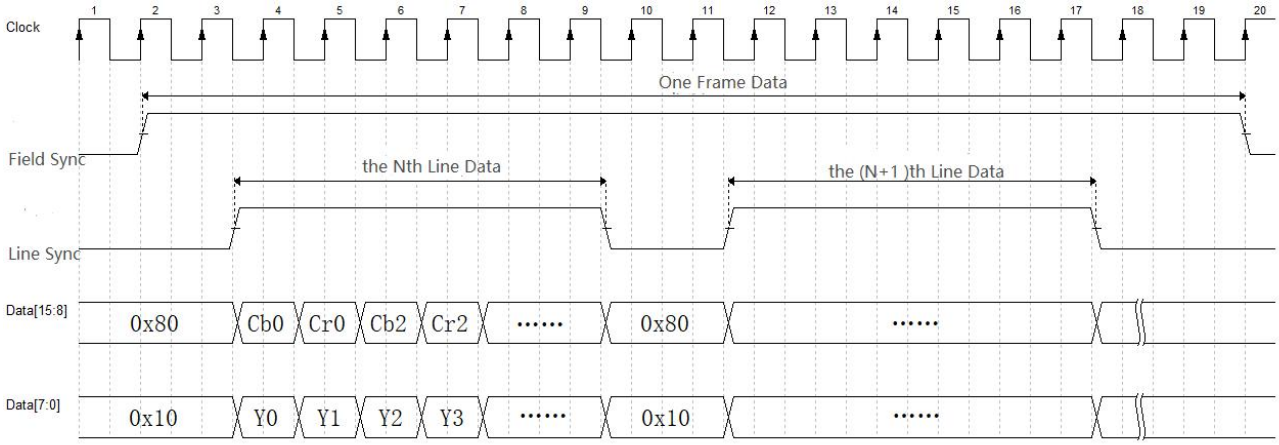

Figure5.2 Timing Chart of BT.1120 External Sync Output

16bit data (high 8bit is chroma data, low 8bit is gray data) is output in the corresponding position of line sync signal. The data output is 0x8010 when the line sync signal is 0.

5.2.2 Timing Introduction of Internal Sync

The reference number is adopted to indicate the start and end of the line or frame in internal sync, see the following Table5.2 for the time sequence of one frame image:

Table5.2 Timing Chart of BT.1120 Internal Sync Output

Invalid line reference code EAV	Blanking 0x8010	Invalid line reference code SAV	Blanking 0x8010
Valid line reference code EAV	Blanking 0x8010	Valid line reference code SAV	Valid data Area The data area size of 640 thermal camera is 640*512
Invalid line reference code EAV	Blanking 0x8010	Invalid line reference code SAV	Blanking 0x8010

The above Table describes format of one frame image which includes valid line, invalid line, blanking and valid data area. The top left corner stands for start of a frame, the bottom right corner stands for end of a frame; the size of one frame, number of invalid line and valid line, the size of blanking area, etc. is decided by the actual status of the thermal camera. All the data in blanking area is 0x8010, every reference number is corresponding to 4 clock periods, and every pixel data is corresponding to one clock period. The reference number and pixel data are all 16bit, see Table 2.3 for the format of the reference code:

Table 5.3 Reference Code Format

	EAV	SAV
Invalid Line	0xFFFF 0x0000 0x0000 0xB6B6	0xFFFF 0x0000 0x0000 0xABAB
Valid Line	0xFFFF 0x0000 0x0000 0x9D9D	0xFFFF 0x0000 0x0000 0x8080

For 16bit data, high 8bit is chroma data, low 8bit is grayscale data in internal sync. The first three clock period of every reference number are 0xFFFF, 0x0000, 0x0000.

Table5.4 BT.1120 CLK Frequency

Model	CLK Frequency
1024	70MHz
1280	90.000MHz

5.3 LVDS_H Video Format

The LVDS_H video output format includes one clock line and four data lines, with no synchronization signals. Sync codes are added to the data to indicate the start or end of a frame or line of data. Unlike other digital video formats, each signal line of the LVDS_H video output provides two bits of data per clock cycle. During the clock's high phase, the video output provides 1 bit of data, and during the clock's low phase, the video outputs the next bit of data.

Users can select from raw data (ORG), non-uniformity corrected data (NUC), denoised data (DNS), or processed image data (DRC) based on their needs. The bit width for raw data (ORG), non-uniformity corrected data (NUC), and denoised data (DNS) is 14 bits, while the bit width for processed image data (DRC) is 10 bits.

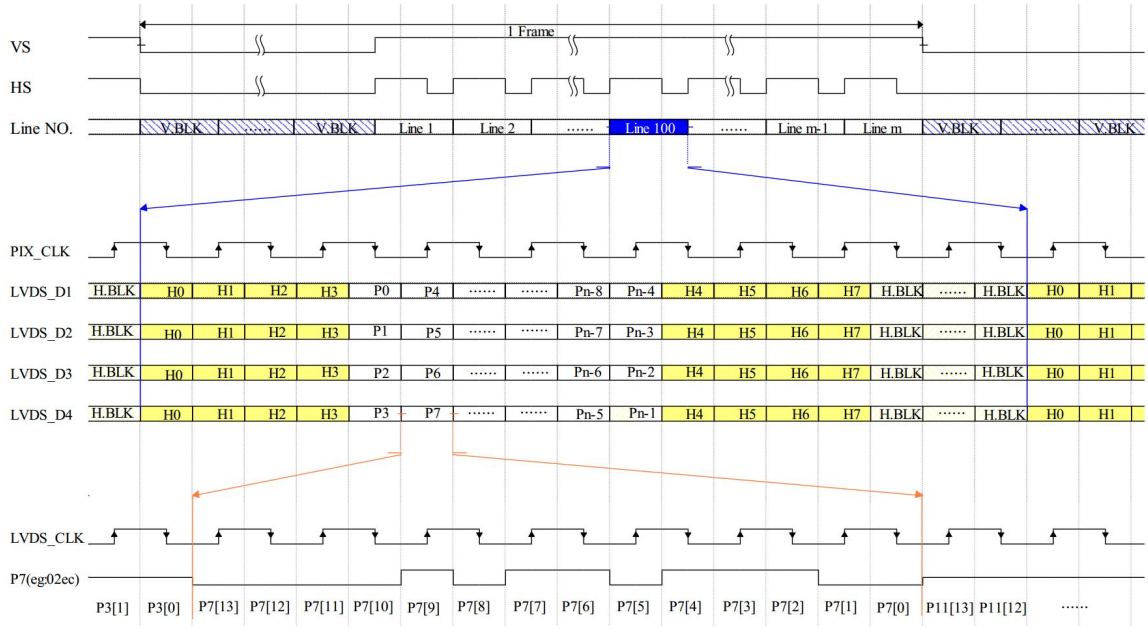

Figure 5.3

In the above Figure 5.3, LVDS_CLK is the signal which is actually used, PIX_CLK signal is only for the reader to understand. For LVDS_CLK, one clock period is corresponding to 2bit data. H0-7 stands for the synchronous code of the video which represents the start and end of a frame or line. The synchronous code of the four channels are the same, H0-3 is SOL, H4-7 is EOL; P stands for pixel data which is arranged in order on 4 data channels; although frame sync signals and line sync signals are marked in the above figure, there is no frame sync and line sync signal in actual LVDS_H video. BLK stands for blanking area, the signal shows 0 in blanking area.

See the following Table 5.5 for sync code in LVDS_H video.

Table5.5 Sync Code in LVDS_H Video

SOF SAV_InValid	Blanking	EOF EAV_InValid
SOL SAV_Valid	Valid data area	EOL EAV_Valid
SOF SAV_InValid	Blanking	EOF EAV_InValid

The format of sync code for LVDS_H video is related to the data bits (10 bit, 12bit and 14bit etc.). The 14bit is used by the module, so the 14bit sync code should be chosen. See the following Table 5.6 for the sync code format of LVDS_H video.

Table5.6 The Sync Code Format of LVDS_H Video

No.		SOL SAV_Valid	EOL EAV_Valid	SOF SAV_InValid	EOF EAV_InValid
H0		All 1	All 1	All1	All1
H1 H2		All 0	All 0	All 0	All 0
H3	10bit	0x200	0x274	0x2AC	0x2D8
	12bit	0x800	0x9D0	0xAB0	0xB60
	14bit	0x2000	0x2740	0x2AC0	0x2D80

We can see from the above illustrations that 1pixel data will be output after 7 clock periods for 14bit data; see the following figure 5.4 for sequence chart of LVDS_H video:

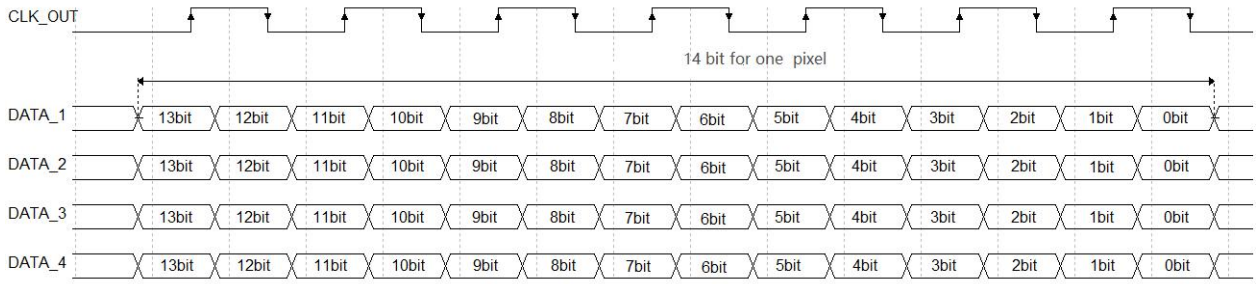

Figure5.4 Timing of LVDS_H

Table5.7 LVDS_H CLK Frequency

Model	CLK Frequency
1024	61.25MHz
1280	78.750MHz

6. Precautions

To protect you and others from injury or to protect your equipment from damage, please read all the following information before using your equipment.

1. The product should not be made towards the sun directly and other high-intensity radiation sources;
2. The optimal environment temperature for operating is - 20 ℃ to 50 ℃;
3. Do not touch or hit the detector window with hands or other objects;
4. Do not touch the equipment and cables with wet hands;
5. Please do not bend or damage cables;
6. Do not scrub your equipment with diluents;
7. Should not unplug and plug other cables without disconnecting the power supply;
8. Wrong cable should not be connected in case that brings damages to the equipment;
9. Please pay attention to prevent static electricity;
10. Please do not disassemble the equipment. If there is any fault, please contact our company, and professional personnel will carry out maintenance.